

Attorney's Docket No. 1207.P004XC6

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

Benjamin S. Ting

Examiner: Not yet assigned

Application No.: Not yet assigned

Art Unit: Not yet assigned

Filed: Herewith

For: ARCHITECTURE AND
INTERCONNECT SCHEME FOR
PROGRAMMABLE LOGIC
CIRCUITS

a Continuation of

Application No.: 10/428,724

Filed: May 1, 2003

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicants.

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Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

 X 37 C.F.R. §1.97(b).

 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

 A statement pursuant to 37 C.F.R. §1.97(e) or

 A check for \$180.00 for the fee under 37 C.F.R. § 1.17(p).

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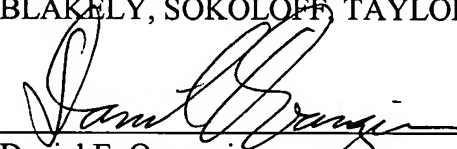
Pursuant to 37 C.F.R. §1.98(d), no copies are enclosed of previously cited art that has been cited in parent application no. 10/428,724, filed May 1, 2003.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 4/21 , 2004


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U.S. PATENT DOCUMENTS

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		Number Code ²	Kind (If known)			
		4,935,734		Austin	6/19/90	
		4,992,680		Benedetti, et al.	2/12/91	
		5,396,126		Britton, et al.	3/7/95	
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		PCT	9410754			5/11/94		
		PCT	9208286			5/14/92		
		EPO	0415542			3/6/91		
		UK	2180382			3/25/87		
		EPO	0630115A2			6/1/94		
		PCT	9504404			2/9/95		
		PCT	9605964			4/3/96		
		PCT	9635261			11/7/96		
		PCT	9428475			12/8/94		
		UK	2295738			5/6/96		

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		5,550,782		Cliff, et al.	8/27/96	
		4,720,780		Dolecek	1/19/88	
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		6,038,627		Plants	3/14/00	
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		5,485,103		Pederson et al.	1/16/96	
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		6,433,580		Ting	8/13/02	

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OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		Cliff, et al., "A Dual Granularity and Globally Interconnected Architecture for A Programmable Logic Device", 9/5/93, IEEE, pp. 7.3.1-7.3.5	
		BRITTON, et al., "Optimized Reconfigurable Cell Array Architecture for High-Performance Field Programmable Gate Arrays," Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, 1993, pp. 7.2.1. - 7.2.5.	
		Xilinx, "The Programmable Gate Array Data Book", 1992.	
		Minnick, R.C., "A Survey of Microcellular Research", vol. 14, no. 2, 4/1967, pp. 203-241.	
		SHOUP, R. G., "Programmable Cellular Logic Arrays," Abstract, Ph.D. Dissertation, Carnegie Mellon University, Pittsburgh, PA, March 1970, (partial) pp. ii-121.	
		SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits," Contract No. AF 19 (628) 2907, Project No. 4645, Task No. 464504, Final Report, November 30, 1965.	
		Wang, P. et al. IEEE, "A High Performance FPGA with Hierarchical Interconnection Structure", pp. 239-242 (May 30, 1994).	
		ATMEL Field Programmable Arrays, AT 6000 Series, 1993, p. 1-16.	
		Motorola Project Brief, "MPA10xx Field Programmable Gate Arrays," September 27, 1993, 4 pages.	
		Altera Corporation Data Sheet, Flex EPF81188 12,000 Gate Programmable Logic Device, September 1992, Ver. 1, pp. 1-20.	

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		Sinan Kaptanoglu, Greg Bakker, Arun Kundu, Ivan Corneillet, Ben Ting, "A New High Density and Very Low Cost Reprogrammable FPGA Architecture", 10 pages, Actel Corporation.	
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		DEVADES, S., et al., "Boolean Decomposition of Programmable Logic Arrays," IEEE 1988, pp. 2.5.1 - 2.5.5.	
		VIDAL, J. J., "Implementing Neural Nets with Programmable Logic," IEEE Transactions on Acoustic, Speech, and Signal Processing, Vol. 36, No. 7, July 1988, pp. 1180-1190.	
		LIU, D.L., et al., "Design of Large Embedded CMOS PLA's for Built-In Self-test," IEEE Transactions on Computed-Aided Design, Vol. 7, No. 1, January 1988, pp. 50-53.	
		SUN, Y., et al., "An Area Minimizer for Floorplans with L-Shaped Regions," 1992 International Conference on Computer Design, 1992 IEEE, pp. 383-386.	
		BURSKY, D., "Fine-Grain FPGA Architecture Uses Four Levels of Configuration Hierarchy," 2328 Electronic Design, 41, No. 20, Cleveland, OH, October 1, 1993, pp. 33-34.	
		F. Zlotnick, P. Butler, W. Li, D. Tang, "A High Performance Fine-Grained Approach to SRAM Based FPGAs", p. 321-326, Wescon September 28-30, 1993.	
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